REMARKS

These remarks are responsive to the Advisory Action dated December 22, 2003. Claims 1-10 are pending in the present application. Claims 1-10 have been rejected. Accordingly, claims 1-10 remain pending.

Applicant includes a Petition for Extension of Time to extend the deadline for filing a response by three (3) months from November 21, 2003 to February 21, 2004.

For the reasons set forth more fully below, Applicant respectfully submits that the present claims are allowable. Consequently, reconsideration, allowance and passage to issue of the present application are respectfully requested.

35 USC §102 Rejections

Independent claims 1, 6, 8, 9, and 10

For ease of discussion independent claims 1, 6, 8, and 9 are provided below for ease of review:

1. (currently amended) A flip-flop comprising:

a first latch for receiving at least one bit;

a second latch coupled to the first latch for storing the at least one bit from the first latch, wherein the size of the second latch is minimized compared to the size of the first latch to reduce power consumption; and

a multiplexor coupled to the first latch and to the second latch for outputting the at least one bit from the first latch when a first clock to the first latch is active and for outputting the at least one bit from the second latch when a second clock to the second latch is active.

6. (currently amended) A flip-flop comprising:

a master latch for receiving at least one bit;

a slave latch coupled to the master latch for storing the at least one bit from the master latch wherein the size of the slave latch is minimized compared to the size of the master latch to reduce power consumption; and

a multiplexor coupled to the master latch and to the slave latch for outputting the at least one bit from the master latch when a first clock to the master latch is active and for outputting the at least one bit from the slave latch when a second clock to the slave latch is active.

8. (previously amended) A method for optimizing power and performance in a flip-flop, wherein the flip-flop includes a first latch and a second latch coupled to the first latch, the method comprising the steps of:

(a) receiving at least one bit into the first latch, wherein the first latch outputs the at least one bit to the second latch and to a multiplexor when a first clock to the first latch is active;

(b) outputting the at least one bit received from the first latch from the multiplexor when the first clock is active; and

(c) outputting the at least one bit received from the second latch from the multiplexor when a second clock to the second latch is active.

9. (currently amended) A flip-flop comprising:

a master latch for receiving at least one bit;

a slave latch coupled to the master latch for storing the at least one bit, wherein the size of the ~~second~~ master latch is minimized compared to the size of the master latch to reduce power consumption; and

a shunt multiplexor coupled to the master latch and to the slave latch for receiving the at least one bit, for outputting the at least one bit from the master latch when a first clock to the master latch is active, and for outputting the at least one bit from the slave latch when a second clock to the slave latch is active.

The Examiner has stated:

> **Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Gregor et al.**
>
> **Note Fig. 2 of Gregor et al, where the master latch is 20, the slave latch is 22 and the MUX is 24. As to the new limitation that the at least one bit is output from the first latch when the first clock is active, and from the second latch when the second latch is active, this is met by Gregor et al, because the first clock is C1 and the second clock is either C2 or the clock received at terminal C of the slave latch 22. The data Q is output from the first latch 20 when the first clock is active and output from the second latch 22 when the second clock is active.**
>
> **Applicant's arguments filed on 7/9/03 have been fully considered but they are not persuasive.**
>
> **As to the argument that "Gregor does not teach or suggest a first latch with a first clock and second latch with a second and independent clock" this argument is not persuasive because the claims do not require that the second clock be independent of the first clock, and, as applicant is well aware, limitations from the specification are not read into the claims.**
>
> **As to the argument that the second latch is not minimized to reduce power consumption, this argument is also not persuasive because nothing in the claims recites that the second is smaller than the first or even what the second latch is minimized with respect to, thus any latch can be broadly interpreted to meet this language. In other words, the latches of Gregor et al are not disclosed as "maximized" in size, so they will inherently be "minimized" with relative to a very large sized (and high power consuming) latch.**

Applicants respectfully disagree.

The present invention as recited in varying scope in amended independent claims 1, 6, 8, and 9 is directed toward a system and method for optimizing power consumption in a flip-flop. The flip-flop comprises a first latch for receiving at least one bit and a second latch coupled to the first latch for storing the at least one bit from the first latch. The size of the second latch is minimized compared to the size of the second latch to reduce power consumption. The flip-flop also comprises a multiplexor for outputting the at least one bit from the first latch when a first clock to the first latch is active and for outputting the at least one bit from the second latch when a second clock to the second latch is active (Summary and Fig. 2B and the accompanying text).

In accordance with present invention, the first clock is used to pass data at a significantly fast rate by outputting data directly from the first latch to the multiplexor. In addition, the

second clock is used to store data in the second latch and later output the data to the multiplexor. Typically, in a slave configuration, the most performance-critical function is the launch time of slave latch (i.e., the second latch). Here, however, the first latch performs the most performance-critical function because it is used to store data. Because the second latch does not serve a performance-critical function, it can be implemented using minimum sized devices to reduce power consumption (Specification generally, Summary). Specifically, the devices with second latch can be one-tenth of the size of the devices in the first latch.

The Gregor Patent

Gregor discloses a scannable double-edge-triggered flip-flop having two latches and a multiplexor, all of which are driven by a single clock. Each latch has a plurality of inputs and is coupled to the clock, which provides a clock signal, via a means for providing a delayed version of the clock signal. The multiplexor has (i) inputs fed by outputs for the latches, and (ii) a select input fed by the clock signal, and means for providing a select signal for selecting the latch whose clock is inactive. Each latch has a scan input gate and a scan output gate, and the scan output of the first latch is applied to the scan input of the second latch to form a scannable latch pair (Abstract and Fig. 2).

First, Gregor does not teach or suggest a second latch coupled to the first latch for storing the at least one bit from the first latch as recited in all of the independent claims. Second, Gregor does not teach or suggest a first latch with a first clock and second latch with a second clock. Thus, the multiplexor of Gregor does not output at least one bit from the first (or master) latch when a first clock to the first (or master) latch is active and for outputting the at least one bit from the second (or slave) latch when a second clock to the second (or slave) latch is active, as

recited in amended independent claims 1, 6, 8, and 9. In contrast, Gregor discloses a single clock to the first and second latches, which selects from the first latch when the clock=0 and selects from the second latch when the clock=1 (column 3, lines 14-16).

Gregor discloses that a single clock drives both of the latches and the multiplexor and that the multiplexor outputs data to both of the first and second latches alternating continuously between both latches as long as the clock cycles. Accordingly, the size of the second latch in Gregor cannot be minimized to reduce power consumption because the second latch performs a performance critical function. Thus, Gregor does not achieve the benefits of a reduction in power consumption as in the present invention.

In the present invention the second (slave) latch does not perform a performance critical function. Thus, the master latch receives the data at a first clock cycle and in the next clock cycle the slave latch receives the data from the master latch. Therefore the size of the second (slave) latch can be minimized compared to the size of the first reduced power consumption.

Therefore, Gregor neither teaches or suggests the invention as recited in independent claims 1, 6, 8, 9, and 10. Accordingly, these claims are allowable over the cited references.

Remaining dependent claims

Dependent claims 2-5, and 7 depend from claims 1 and 6, respectively. Accordingly, the above-articulated arguments related to claims 1 and 6 apply with equal force to claims 2-5, and 7 and are thus allowable over the cited references for at least the same reasons as claims 1 and 6.

Conclusion

In view of the foregoing, Applicants submit that claims 1-10 are patentable over the cited references. Applicants, therefore, respectfully request reconsideration and allowance of the claims as now presented.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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Date

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